REMARKS

Claim Rejections – 35 U.S.C. § 102/103

The Examiner has rejected claims 1 and 2 under 35 U.S.C. § 102(e) as being anticipated by Pramanick et al. (US Patent 6,117,770, of record). The Examiner has rejected claims 3-4 and 7 under 35 U.S.C. § 103(a) as being unpatentable over Pramanick et al. (US Patent 6,117,770) in view of Akutsu et al. (US Patent 4,749,584, of record). The Examiner has rejected claims 5 and 6 under 35 U.S.C. §103(a) as being unpatentable over Pramanick et al. (US Patent 6,117,770, of record). The Examiner has rejected claims 18-19 and 21 under 35 U.S.C. § 103(a) as being unpatentable over Nogami et al. (US Patent 6,022,808) in view of Pramanick et al. (US Patent 6,117,770, of record). The Examiner has rejected claim 20 under 35 U.S.C. § 103(a) as being unpatentable over Nogami et al. (US Patent 6,022,808) in view of Pramanick et al. (US Patent 6,117,770, of record) and further in view of Akutsu et al. (US Patent 4,749,584, of record).

It is Applicant's understanding that the cited references either alone or in combination fail to teach or render obvious Applicant's invention as claimed in claims 1, 3-7 and 18-21.

With respect to claim1, 3 and 4, Applicant teaches and claims a method of forming hardened interconnects. According to Applicant's invention, a metal layer comprising copper and additional metal species are co-deposited over a semiconductor wafer surface. After depositing the metal layer comprising copper and the additional metal species, the metal layer is chemically mechanically polished. The additional metal species harden the copper layer to reduce the rate of polishing of the copper. Applicant understands Pramanick et al. as disclosing

forming a barrier layer 122 and a copper layer 101 in an opening formed in an insulating layer 202 and on top of the insulating layer 202. The copper layer 101 on top of the barrier layer 122 on top of the insulating layer 202 is then polished back until the copper layer 101 is planar with the barrier layer 122 as shown in Figure 2. After the copper layer 101 is polished back, dopants 206 are implanted into the copper layer 101 in the opening as well as into the barrier layer 122 (Figure 3). Next, the barrier layer 122 is polished back to reveal insulating layer 202. Thus, in Pramanick, the copper layer 101 is polish back prior to introducing the dopants 206. In Pramanick, dopants 206 are not present in the copper layer while polishing the copper layer as claimed by Applicant. As such, Pramanick clearly fails to teach or render obvious Applicant's invention as claimed in claims 1, 3 and 4. As such, Applicant respectfully, requests the removal of the 35 U.S.C. 102 and 103 rejections of claims 1, 3 and 4 and seeks an early allowance of these claims.

With respect to claim 5-7, Applicant teaches and claims a method of forming hardened interconnects comprising depositing metal layers over a semiconductor wafer; introducing additional metal species; heating the deposited metal film with the introduced metal species; allowing the heated metal to cool, so as to form precipitates of said introduced metal species; and "**after allowing said heated metal film to cool**" performing chemical mechanical polishing wherein said additional metal precipitants harden said deposited metal layer to reduce the rate of polishing.

Applicant understands Akutsu et al. to disclose heating the semiconductor wafer 200 to activate the implant element to drive it into the copper after the polishing of the copper layer 101 and the barrier layer 122 (see Col. 5, lines 35-43). Thus, Pramanick et al. fails to teach polishing a metal layer after heating the metal layer as claimed by Applicant. As such, Applicant respectfully, requests the removal

of the 35 U.S.C. 102 and 103 rejections of claims 5-7 and seeks an early allowance of these claims.

With respect to claims 18-21, Applicant claims a method of forming interconnects of an integrated circuit comprising forming an opening in an insulating film over a substrate. Then co-depositing a metal film and an additional metal species over said insulating layer and in said opening and filling said opening with said metal film and said additional species. After co-depositing said metal film and said additional metal species to fill said opening, the co-deposited metal film with the additional species is removed from over the top surface of the insulating film by chemical mechanical polishing.

Applicant understands Nogami et al. as describing to form an barrier layer 12 in an opening and on top of an insulating layer 10. Next, an undoped copper layer 13 is formed over the barrier layer 12 on top of the insulating layer 10 and over the barrier layer in the opening formed in the insulating layer 10. Next, a doped layer of copper 14 is formed over the top surface of the undoped copper layer 20 (Figure 1). Next, as shown in Figure 2, the substrate is annealed to drive the dopants in doped copper layer 14 into the undoped copper layer 13 to produce a doped copper layer 20 inside the via opening formed in the insulating layer 10. Chemical mechanical polishing is then used to remove the deposited doped copper layer 14 and the diffusion doped copper layer 20 (Figure 3). Thus, Nogami et al. fails to teach co-depositing a metal film and an additional metal species into an opening formed in an insulating layer as claimed by Applicant. In Nogami, an undoped copper layer 13 is deposited into the opening in the insulating layer 10. Copper layer 13 in the opening in the insulating layer 10 is doped after deposition and not co-deposited.

As such, for the above mentioned reasons, it is Applicant's understanding that cited references fail to teach or render obvious Applicant's invention as claimed

in claims 18-21. As such, Applicant respectfully, requests removal of the 35 U.S.C. 103 rejections of claims 18-21 and seeks an early allowance of these claims.